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**RESPONSE UNDER 37 C.F.R. 1.116 EXPEDITED  
PROCEDURE EXAMINING GROUP 2823**

Attorney Docket No.: 5649-1225

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re: Byeong-chan Lee et al. Confirmation No.: 6744  
Serial No.: 10/722,193 Group Art Unit: 2823  
Filed: November 26, 2003 Examiner: Brook Kebede  
For: INTEGRATED CIRCUIT DEVICES HAVING BURIED INSULATION  
LAYERS AND METHODS OF FORMING THE SAME

February 13, 2006

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**AMENDMENT AFTER FINAL**

Sir:

Responsive to the Final Office Action dated December 13, 2005, please amend the above-identified application as shown. It is not believed that an extension of time and/or additional fee(s), including fees for additional claims, are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

**Amendments to the Claims** are reflected in the listing of claims, which begin on page 2 of this paper.

**Remarks/Arguments** begin on page 6 of this paper.

*3/3/06*

*BR*

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